CLAIMS

[0083] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a semiconductor structure, comprising the steps of:

providing a conductive layer over a semiconductor substrate;

forming at least one capacitor electrode adjacent said conductive layer; and

subsequently forming a silicide layer over at least said conductive layer.

2. The method of claim 1, wherein said silicide layer is formed over said conductive layer and said capacitor electrode.

3. The method of claim 1, further comprising the step of providing a dielectric layer over said conductive layer.

4. The method of claim 3, wherein said step of forming at least one capacitor electrode comprises forming a polysilicon layer over said dielectric layer.

5. The method of claim 4, wherein said polysilicon layer is formed by deposition at a temperature between about 600°C to about 800°C.

6. The method of claim 1, wherein said step of forming a silicide layer includes providing a metal layer over at least said conductive layer and annealing said metal layer to form said silicide layer.

7. The method of claim 6, wherein said metal layer is formed of a material selected from the group consisting of tungsten, titanium, cobalt, tantalum, molybdenum and platinum.

8. The method of claim 1, wherein said semiconductor structure is a gate of an MOS transistor.

9. A method of reducing migration of impurity atoms between two gate structures of a DRAM device, comprising the steps of:

forming at least one in-pixel gate structure in an array region of a substrate, said at least one in-pixel gate structure being further formed by providing a first doped conductive layer over said substrate and providing a first silicide region over said first doped conductive layer;

forming at least one peripheral gate structure in a peripheral region of said substrate, said peripheral region being adjacent said array region, said at least one peripheral gate structure being further formed by providing a second doped conductive layer over said substrate and providing a second silicide region over said second doped conductive layer; and

forming at least one capacitor structure over an isolation region in said array region, said at least one capacitor structure being further formed by providing a first capacitor electrode layer, providing a dielectric layer over said first capacitor electrode layer, and providing a second capacitor electrode layer over said dielectric layer, wherein said steps of providing said first and second silicide regions are conducted subsequent to said step of providing said second capacitor electrode layer.

10. The method of claim 9, wherein said first and second doped conductive layers are formed of polysilicon.

11. The method of claim 9, wherein said second capacitor electrode layer is formed of doped polysilicon.

12. The method of claim 11, wherein said undoped polysilicon is formed by deposition at a temperature between about 600°C to about 800°C.

13. A method of forming a memory cell, comprising the steps of:

forming a transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate, said step of forming said transistor including providing a silicide region of said gate; and

forming a capacitor adjacent said transistor by providing a first conductive layer, a dielectric layer and a second conductive layer, wherein said steps of providing said first conductive layer, said dielectric layer and said second conductive layer are conducted prior to said step of providing said silicide region of said gate.

14. The method of claim 13, wherein said first conductive layer is formed of doped polysilicon.

15. The method of claim 13, wherein said second conductive layer is formed of undoped polysilicon.

16. The method of claim 15, wherein said second conductive layer is formed by deposition at a temperature between about 600°C to about 800°C.

17. The method of claim 13, wherein said step of providing said silicide region of said gate includes providing a metal layer a gate electrode and annealing said metal layer to form said silicide layer.

18. The method of claim 13, wherein said transistor is a MOSFET.

19. The method of claim 13, wherein said semiconductor substrate is a silicon substrate.

20. The method of claim 13, wherein said memory cell is a DRAM.

21. The method of claim 13, wherein said memory cell is one of a DRAM, flash memory or SRAM.

22. A method of forming an imaging device having at least a gate structure with decreased impurity migration, comprising the steps of:

forming at least one photosensor in a substrate;

forming a first conductive layer over said substrate;

forming a capacitor structure by providing a dielectric layer over said first conductive layer, and providing a second conductive layer over said dielectric layer; and

subsequently providing a silicide layer over said first conductive layer and said capacitor structure.

23. The method of claim 22, wherein said imaging device is one of a 3T, 4T, 5T, 6T or 7T imaging device.

24. The method of claim 22, wherein said imaging device is a CMOS imager.

25. The method of claim 22, wherein said imaging device is a CCD imager.

26. The method of claim 22, wherein said first conductive layer is formed of doped polysilicon.

27. The method of claim 22, wherein said second conductive layer is formed of a material selected from the group consisting of a polysilicon, polysilicon/WSi and polysilicon/WN/W.

28. The method of claim 22, wherein said second conductive layer is formed of polysilicon.

29. The method of claim 28, wherein said second conductive layer is formed by deposition at a temperature between about 600°C to about 800°C.

30. The method of claim 22, wherein said step of providing said silicide layer includes providing a metal layer and annealing said metal layer to form said silicide layer.

31. The method of claim 22, wherein said dielectric layer is formed of a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, and BST.

32. A DRAM, comprising:

at least a gate structure formed over a substrate, said gate structure comprising a first conductive layer and a first region of a silicide layer over said first conductive layer; and

at least one capacitor adjacent said gate structure, said capacitor comprising a first capacitor electrode, a dielectric layer, a second capacitor electrode and a second region of said silicide layer over said second capacitor electrode.

33. The DRAM of claim 32, wherein said gate structure further comprises a gate oxide layer.

34. The DRAM of claim 32, wherein said first conductive layer is formed of doped polysilicon.

35. The DRAM of claim 32, wherein said first capacitor electrode is formed of doped polysilicon.

36. The DRAM of claim 32, wherein said second capacitor electrode is formed of doped polysilicon.

37. The DRAM of claim 32, wherein said dielectric layer is formed of a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, and BST.

38. An imaging device, comprising:

a substrate;

at least one photosensor in said substrate;

at least one in-pixel gate structure formed in an active region of said substrate, said at least one in-pixel gate structure comprising a first conductive layer and a first region of a silicide layer over said first conductive layer; and

at least one capacitor formed over an isolation region adjacent said active region and a peripheral region of said substrate, said at least one capacitor comprising a first capacitor electrode, a dielectric layer, a second capacitor electrode and a second region of said silicide layer over said second capacitor electrode.

39. The imaging device of claim 38, wherein said at least one in-pixel gate structure further comprises a gate oxide layer.

40. The imaging device of claim 38, wherein said first conductive layer is formed of doped polysilicon.

41. The imaging device of claim 38, wherein said first capacitor electrode is formed of doped polysilicon.

42. The imaging device of claim 38, wherein said second capacitor electrode is formed of undoped polysilicon.

43. The imaging device of claim 38, wherein said dielectric layer is formed of a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, and BST.

44. A CMOS imager system, comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a semiconductor substrate;

at least one photosensor in said substrate;

at least one gate structure formed in an array region of said substrate, said at least one gate structure comprising a first conductive layer and a first region of a silicide layer over said first conductive layer; and

at least one capacitor adjacent said gate structure, said at least one capacitor comprising a first capacitor electrode, a dielectric layer, a second capacitor electrode and a second region of said silicide layer over said second capacitor electrode.

45. A CCD imaging device, comprising:

a semiconductor substrate;

at least one photosensor in said semiconductor substrate;

at least one in-pixel gate structure formed in an active region of said substrate, said at least one in-pixel gate structure comprising a first

conductive layer and a first region of a silicide layer over said first conductive layer; and

at least one capacitor formed over an isolation region, said isolation region being adjacent said active region and a peripheral region of said substrate, said at least one capacitor comprising a first capacitor electrode, a dielectric layer, a second capacitor electrode and a second region of said silicide layer over said second capacitor electrode.